REMARKS

The Official Action dated July 15, 2004 has been received and its contents carefully noted. In view thereof, independent claim 6 has been amended in order to better define that which Applicants regard as the invention. Additionally, claims 13, 14 and 22 have been cancelled. Accordingly, claims 1-10, 12, 15 and 21, 23 and 24 are presently pending in the instant application with claims 1-5 being withdrawn from further consideration by the Examiner.

Referring now to the Official Action, and particularly page 2 thereof, claims 6-10, 12-14 and 21-24 are rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,923,987 issued to Burr in view of U.S. Patent No. 5,786,620 issued to Richards, Jr. et al. This rejection is respectfully traversed in that the combination provided in the Office Action neither discloses nor remotely suggests that which is now set forth by Applicants' claimed invention.

The Burr patent is directed to a method of making asymmetric low power MOS devices (see Abstract).

The Richards Jr. patent is directed to a Fermi-FET that includes a drain extension region of the same conductivity type as the drain region and a drain pocket implant region of opposite conductivity type from the drain region (see Abstract).

On the other hand, the present invention is directed to a method for fabricating a semiconductor device. In the method, a gate electrode is formed over a semiconductor region with the gate insulating film interposed therebetween. Heavy ions are implanted into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask. A first ion implanted layer of a second conducitivity, where at least an upper part of which is an amorphous layer, is formed. Ions of a first dopant are implanted into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of a first conductivity type. A first annealing process is conducted to activate the first and second ion implanted layers, thereby forming an extended high concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer of the second conductivity type which is in contact with a bottom portion of the extended high concentration dopant diffused layer through diffusion of the heavy ions.

A dislocation loop layer is formed in the lower region of the amorphous layer in the semiconductor region in the when the heavy ions are implanted. The pocket dopant diffused layer is formed, in the first annealing process, having a peaked dopant concentration produced by trapping heavy ions in the dislocation loop layer, the pocket dopant diffused layer and the extended high concentration dopant diffused layer being in contact at the peak dopant concentration of the pocket dopant diffused layer, and a side of the extended high concentration dopant diffused layer, located below the gate electrode, is not covered by the pocket dopant diffused layer. Additionally, the heavy ions are indium ions, and an implant dose of the indium ions is more than $5x10^{13}/cm^2$.

That is, as the Examiner can readily appreciate from independent claim 6, the heavy ions are indium ions, and an implant dose of the indium ions is more than $5x10^{13}/cm^2$ to form an amorphous layer and a dislocation loop layer in the semiconductor region. Additionally, the pocket dopant diffused layer is formed having a peak dopant concentration produced by trapping heavy ions in the dislocation loop layer and the pocket dopant diffused layer and the extended high-concentration dopant diffused layer are in contact at the peak dopant concentration of the pocket dopant diffused layer. It is respectfully submitted that the combination proposed by the Examiner fails to disclose or remotely suggest these features.

For example, neither Burr nor Richards Jr. disclose or suggest that the heavy ions are indium ions, and that an implant dose of the indium ions is more than $5x10^{13}/cm^2$ as now recited in independent claim 6. Instead, Burr discloses that boron is implanted at about 5×10^{12} **to** 5×10^{13} $/cm^2$ to form the asymmetric pocket region 116 (see columns 11 and 12 and corresponding Figs. 4G to 4J). Moreover, while Burr states that indium may be used as a dopant implanted into the asymmetric pocket region 116 for NFETs, the Burr disclosure fails to disclose any specific implant conditions associated with indium. Applicants note that the mass number of boron is different from that of indium and that, if the implant conditions employed by Burr for boron were to be used as the implant conditions for indium, the resulting dopant profile would be entirely different from the desired dopant profile (as suggested in column 11, lines 63-67). Accordingly, Applicants respectfully submit that Burr while generally disclosing indium as an implant, certainly does not disclose or suggest that the dose is more than $5x10^{13}/cm^2$ as now recited in independent claim 6. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection.

With respect to paragraph 3 of the Office Action, claim 15 has been rejected under

35 U.S.C. §103(a) as being unpatentable over Burr as applied to claim 6 above and further in view of U.S. Patent No. 5,399,506 issued Tsukamoto. This rejection is likewise respectfully traversed in that the patent to Tsukamoto fails to overcome the aforementioned shortcomings associated with the combination of Richards, Jr. and Burr.

As discussed previously, while the patent to Tsukamoto may teach that RTA processes are well known in the art, it is respectfully submitted that Tsukamoto fails to overcome the significant shortcomings associated with the combination proposed by the Examiner as discussed in detail hereinabove. Accordingly, it is respectfully submitted that Applicants' claimed invention as set forth in dependent claim 15 which includes all of the limitations of independent claim 6 clearly distinguishes over the combination proposed by the Examiner.

Therefore, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 6-10, 12, 15 and 21, 23, 24 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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